ŀⱨN

# UNITED STATES PATENT AND TRADEMARK OFFICE

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/032,144 | 12/20/2001 | Patrice Roussel | 10559-644001 / P12488 | 3547 |

| | | |
|---|---|---|
| 20985 7590 11/29/2005 | | EXAMINER |
| FISH & RICHARDSON, PC | | MEONSKE, TONIA L |
| P.O. BOX 1022 | | |
| MINNEAPOLIS, MN 55440-1022 | ART UNIT | PAPER NUMBER |
| | 2181 | |

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>09 September 2005</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) <u>19-23,73-76 and 83-92</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>19-23, 73-76, and 83-92</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>06 June 2002</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1.      The drawings are objected to under 37 CFR 1.83(a).  The drawings must show every feature of the invention specified in the claims.  Therefore "loading a plurality of groups of bits from a source into a plurality of non-contiguous groups of bits of a destination register and duplicating the plurality of non-contiguous groups of bits in the destination register into subsequent groups of bits in the destination register" in claim 19, and similarly in claims 73, 83, and 88, must be shown or the feature(s) canceled from the claim(s).  No new matter should be entered.

2.      Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

## *Claim Rejections - 35 USC § 102*

3.      The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.      Claims 19, 20, 22, 83, 84, 86, 88, 89, and 91, are rejected under 35 U.S.C. 102(b) as

being clearly anticipated by Sidwell et al., European Patent Application EP 0 743 594 A1, cited

on the information disclosure statement filed on June 9, 2003 (herein referred to as Sidwell).

5.      Referring to claim 19, Sidwell has taught a method executed in a processor comprising:

**a.**      loading a plurality of groups of bits from a source into a plurality of non-

contiguous groups of bits of a destination register (Figure 17, see zip2n4v2p, For the

purpose of this rejection, the source is V3/V2/V1/V0, then the zip2n4v2p instruction is

performed on the source to produce a destination V2/V2/V0/V0. The bits in source

groups V1 and V0 are loaded into the first location and the third location of the

destination memory.); and

**b.**      duplicating the plurality of non-contiguous groups of bits in the destination

register into subsequent groups of bits in the destination register (Figure 17, see

zip2n4v2p, the V2 bits in the first destination memory location are duplicated into the

second destination memory location, and the V0 bits in the third destination memory

location are duplicated into the fourth destination memory location.).

6.      Referring to claim 20, Sidwell has taught the method of claim 19, as described above, in

which the source is an extended multimedia register (Figure 6, element 104).

7.      Referring to claim 22, Sidwell has taught the instruction of claim 19, as described above, and in which the source is a memory location (Figure 17, V3/V2/V1/V0, Figure 1, element 4).

*8.*     Referring to claim 83, Sidwell has taught a computer instruction comprising:

    a.      a load and duplicate instruction (Figure 17, zip2n4v2p) that causes a processor to load a plurality of groups of bits from a source into a plurality of non-contiguous groups of bits of a destination register and duplicate the plurality of non-contiguous groups of bits in the destination register into subsequent groups of bits in the destination register (Figure 17, see zip2n4v2p, For the purpose of this rejection, the source is V3/V2/V1/V0, then the zip2n4v2p instruction is performed on the source to produce a destination V2/V2/V0/V0. The bits in source groups V1 and V0 are loaded into the first location and the third location of the destination memory. The V2 bits in the first destination memory location are duplicated into the second destination memory location, and the V0 bits in the third destination memory location are duplicated into the fourth destination memory location.).

9.      Claims 84 and 86 are rejected for the same reasons as set forth in claims 20 and 22, respectively.

10.     Claim 88 is rejected for the same reasons as claim 83.

*11.*    Claims 89 and 91 are rejected for the same reasons as set forth in claims 20 and 22, respectively.

### *Claim Rejections - 35 USC § 103*

12.     The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13.	Claims 21, 23, 73-76, 85, 87, 90, and 92 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sidwell et al., European Patent Application EP 0 743 594 A1, cited on the information disclosure statement filed on June 9, 2003 (herein after Sidwell).

14.	Referring to claim 21, Sidwell has taught the method of claim 20, as described above. Sidwell has not taught wherein the extended multimedia register is configured as a double floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The loading would be performed the same regardless of the configuration of the data type. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the memory location be configured to store any type of data, including double floating point, because merely labeling the data differently from that in the prior art would have been obvious. See Gulack cited above.

15.	Referring to claim 23, Sidwell has taught the method of claim 22, as described above. Sidwell has not taught in which the memory location is configured as a double floating point data type. However, these differences are found only in the nonfunctional descriptive material. This descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see in re Gulack, 703 F .2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re

Lowry, 32 F .3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Therefore it would have been obvious

to one of ordinary skill in the art at the time the invention was made to have the memory location

be configured store any type of data because merely labeling the data differently from that in the

prior art would have been obvious. See Gulack cited above.

16.     Referring to claim 73, Sidwell has taught a processor comprising:

    a.      basic program registers (Figure 1, element 12);

    b.      an address space (Figure 1, page 3);

    c.      a source (Figure 17, V3/V2/V1/V0);

    d.      a destination register (Figure 17, V2/V2/V0/V0); and

    e.      logic to load a plurality of groups of bits of the source into a plurality of non-

contiguous groups of bits in the destination register and duplicate the plurality of non-

contiguous groups of bits into subsequent groups of bits in the destination register (Figure

17, see zip2n4v2p, For the purpose of this rejection, the source is V3/V2/V1/V0, then the

zip2n4v2p instruction is performed on the source to produce a destination V2/V2/V0/V0.

The bits in source groups V1 and V0 are loaded into the first location and the third

location of the destination memory. The V2 bits in the first destination memory location

are duplicated into the second destination memory location, and the V0 bits in the third

destination memory location are duplicated into the fourth destination memory location.).

17.     Sidwell has not specifically taught registers that are labeled "floating point unit".

However, these differences are found only in the nonfunctional descriptive material. This

descriptive material will not distinguish the claimed invention from the prior art in terms of

patentability, see in re Gulack, 703 F .2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re

Lowry, 32 F .3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the registers be any type of registers, including floating point unit registers, because merely labeling the registers differently from that in the prior art would have been obvious. See Gulack cited above.

18.     Referring to claim 74, Sidwell has taught the instruction of claim 73, as described above, Sidwell has not taught the source representing a double floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The loading would be performed the same regardless of the type of data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983)l In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source represent any type of data, including double floating point, because merely labeling the type differently from that in the prior art would have been obvious. See Gulack cited above.

19.     Referring to claim 75, Sidwell has taught the processor of claim 73, as described above, and in which the source register is in a memory location (Figure 1, element 4). Sidwell has not taught in which the source register represents a double floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The loading would be performed the same regardless of the type of data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983)l In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Therefore it would have

been obvious to one of ordinary skill in the art at the time the invention was made to have the

registers represent any type of registers, including double floating point, because merely labeling

the registers differently from that in the prior art would have been obvious. See Gulack cited

above.

20.      Referring to claim 76, Sidwell has taught the processor of claim 73, as described above,

and in which the destination register is an extended multimedia register (Figure 6, element 104).

*21.*      Claims 85 and 87 are rejected for the same reasons as set forth in claims 21 and 23

respectively.

*22.*      Claims 90 and 92 are rejected for the same reasons as set forth in claims 21 and 23

respectively.

### *Response to Arguments*

*23.*      Applicant's arguments with respect to claims 19-23,73-76 and 83-92 have been

considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

24.      Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

25.      A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.
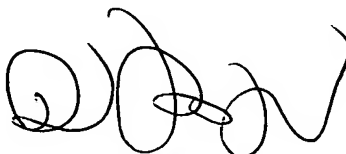
26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

DOV POPOVICI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100